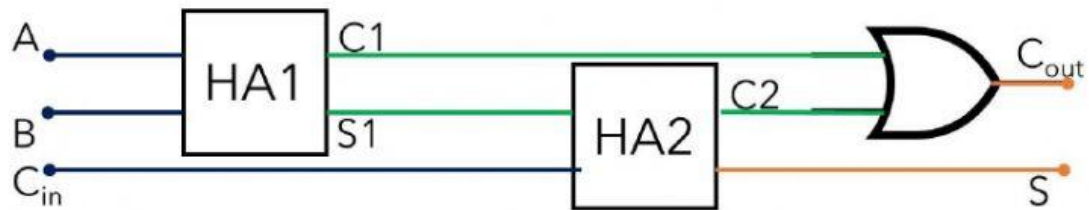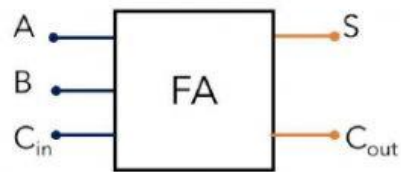Complete the truth table for this single bit full adder circuit constructed from 2 half adders and an OR gate.

A	B	C_{in}	C1	S1	C2	C_{out}	S
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					