**NAME:..... DATE:.....**

**PTES 9618 Computer Science Worksheet** **VON NEUMANN ARCHITECTURE**

**Source: 9618_w24_qp_33.pdf (Page 3)**

**2** Reduced Instruction Set Computers (RISC) is a type of processor.

Identify **four** features of a RISC processor.

1 .....

.....

2 .....

.....

3 .....

.....

4 .....

.....

[4]

**Source: 9618_w24_qp_32.pdf (Page 10)**

**8** Complex Instruction Set Computer (CISC) is a type of processor.

Identify **four** features of a CISC processor.

1 .....

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2 .....

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3 .....

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4 .....

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[4]

LIVEWORKSHEETS

**Source: 9618_s24_qp_33.pdf (Page 11)**

**11** Reduced Instruction Set Computers (RISC) and Complex Instruction Set Computers (CISC) are two types of processor.

**(a)** State **two** features of RISC processors.

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..... [2]

**(b)** Outline the process of interrupt handling as it could be applied to RISC or CISC processors.

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..... [3]

**(c)** Explain how pipelining affects interrupt handling for RISC processors.

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..... [3]

LIVEWORKSHEETS

Source: 9618_s22_qp_32.pdf (Page 8)

**5** There are four basic categories of computer architecture. Single Instruction Single Data (SISD) is one architecture.

Identify the **three other** categories of computer architecture.

Describe each category that you identify.

Architecture 1 .....

Description .....

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Architecture 2 .....

Description .....

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Architecture 3 .....

Description .....

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.....

.....

[6]

LIVEWORKSHEETS

Source: 9618_s26_qp_33.pdf (Page 4)

4 (a) Describe the characteristics of massively parallel computers.

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..... [3]

(b) State **one** difference and **one** similarity between the SIMD and MISD computer architectures.

difference .....

.....

.....

similarity .....

.....

.....

[2]

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10 Describe the features of the SIMD and MISD computer architectures.

SIMD .....

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.....

.....

MISD .....

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.....

[4]

LIVEWORKSHEETS

Source: 9618_s22_qp_11.pdf (Page 12)

6 **(a)** A computer system is designed using the basic Von Neumann model.

**(i)** Describe the role of the registers in the Fetch-Execute (F-E) cycle.

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..... [5]

**(ii)** Describe when interrupts are detected in the F-E cycle **and** how the interrupts are handled.

Detected .....

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Handled .....

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[5]

8 A computer designed using the Von Neumann model for a computer system contains general purpose registers and special purpose registers.

**(a)** Describe the purpose of the Status Register (SR).

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..... [2]

LIVEWORKSHEETS

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**(b)** Identify **two** differences between general purpose registers and special purpose registers.

1 .....

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2 .....

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[2]

Source: 9618_w23_qp_11.pdf (Page 9)

**5** The Central Processing Unit (CPU) of the basic Von Neumann model for a computer system contains several special purpose registers.

**(a)** The Memory Data Register (MDR), Index Register (IX) and the Accumulator (ACC) are examples of special purpose registers.

Identify **two other** special purpose registers **and** state their role in the CPU.

Special purpose register 1 .....

Role .....

.....

.....

Special purpose register 2 .....

Role .....

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.....

[4]

**(b)** Describe what is meant by the **Immediate Access Store (IAS)** in a computer system.

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..... [2]

LIVEWORKSHEETS

**Source: 9618_w22_qp_11.pdf (Page 10)**

5 **(a)** State what is meant by the **stored program concept** in the Von Neumann model of a computer system.

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..... [1]

**(b)** A Central Processing Unit (CPU) contains several special purpose registers and other components.

**(i)** State the role of the following registers.

Program Counter (PC) .....

.....

.....

Index Register (IX) .....

.....

.....

Status Register (SR) .....

.....

.....

[3]

**(ii)** Tick (✓) **one** box in each row to identify the system bus used by each CPU component.

| CPU component | Data bus | Address bus | Control bus |
|---|---|---|---|
| System clock | | | |
| Memory Address Register (MAR) | | | |

[1]

**(iii)** Describe the purpose of the Control Unit (CU) in a CPU.

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..... [2]

LIVEWORKSHEETS