Fill-In-The-Blank Quiz (DRAG & DROP)

Fill in each blank with the most appropriate word selected from the Answer Bank below. Each word may be used once or unused.

pipelining	*Micro coding*	*code size*	*pipeline hazards*
Random Access Memory	*power consumption*	*thermal heat*	*Address Bus*
Main Memory	*general-purpose registers*	*compiler*	*hardwired*

1	A major benefit of RISC processors is their highly effective implementation of _____, which is made possible because every instruction has a fixed length and takes one clock cycle.	
2	The primary drawback of choosing a RISC architecture is that the program's compiled binary machine code will have a larger compared to an equivalent CISC program.	
3	CISC architectures minimize code footprint because instructions can access operands directly via _____, avoiding separate load and store stages.	
4	A key limitation of CISC processors in mobile applications is high ____, caused by the continuous power required to operate complex internal decoding circuitry.	
5	RISC processors require a larger number of to temporarily store data values, compensating for the inability to perform math operations directly of memory.	
6	In terms of system development, RISC shifts structural complexity away from hardware design and moves it into the software development phase.	
7	A distinct benefit of CISC instructions is that they allow developers to write shorter assembly programs that use less _____ to store code.	
8	A limitation of pipelines, a CISC architecture is the frequent occurrence of ____ , it happens when an instruction takes a variable number of clock cycles and delays subsequently.	
9	Because RISC instructions are optimized for a single clock cycle, their hardware decoder is typically _____ , using logic gates directly instead of relying on microcode lookups.	
10	When choosing a processor for a low-power, embedded smart appliance, an engineer would select a RISC chip because its simpler hardware design generates less _____.	

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