

Draw lines in between to match the answer

RISC vs CISC Processors

Terminology	Definitions
RISC Architecture	An abstract configuration boundary containing the complete collection of binary machine commands that a specific CPU family can interpret and process.
CISC Architecture	A physical execution logic circuit format directly embedded in silicon layout using combinations of gates to achieve maximum instruction throughput without lookups.
General-Purpose Registers	A hardware optimization layout that concurrently overlaps separate instruction processing cycles across unique sub-stages like Fetch, Decode, and Execute.
Pipelining	An internal hardware control component responsible for breaking down variable-length macro instructions into manageable execution routing logic signals.
Instruction Set Architecture (ISA)	A processor layout philosophy dedicated to maximizing complex operational capabilities directly inside physical hardware layers to minimize raw assembly line counts.
Compiler	High-speed internal CPU workspace units required in extensive quantities by register-to-register structures to support intermediate computation steps.
Pipeline Hazard	A functional architectural design pattern requiring explicit memory retrieval operations to isolate CPU processing exclusively inside register rows.
Register-to-Register Model	A structural error or delay state occurring inside instruction lines when target arguments or control jumps conflict with ongoing uncompleted sequence pipelines.
Complex Internal Control Unit	A software parsing tool that bears the heavy burden of optimizing macro application syntax down into safe, fast sequences of simple atomic machine steps.
Hardwired Control Unit	A design philosophy centering on uniform instruction execution shapes mapped closely to brief, single-cycle timing intervals to accelerate step pacing.