Classification: Internal

B2 LISTENING PRACTICE 9

Part 1. Verification-based Projects

Listen and choose the correct answer A, B, or C.

1. What can you do for level 1 verification-based projects?

A. develop a complete test bench testing a synchronous FIFO

B. write test benches to the already discussed RTL projects

C. implement UVM based test bench for AXI interface

2. What should the test bench cover?

A. every possible condition

B. AXI interface

C. RISC-V processor

3. What can you develop for level 2?

A. a complete test bench testing a synchronous FIFO

B. UVM based test bench for AXI interface

C. formal verification of RISC-V processor

4. What can you implement for level 3 verification projects?

A. test benches to the already discussed RTL projects

B. a complete test bench testing a synchronous FIFO

C. UVM based test bench for AXI interface

5. What else can you do for level 3 verification projects?

A. formal verification of RISC-V processor

B. develop a complete test bench testing a synchronous FIFO

C. write test benches to the already discussed RTL projects

Part 2. Backend / Physical Design

Listen and write ONE WORD ONLY for each answer.

Physical Design

The final convergence happens for area, power and (1) _____.

Level 1 project:

- make a NAND gate
- implement → (2) _____

Level two:

LIVEWORKSHEETS

- Physically implement any of the designs mentioned for RTL design
- To concentrate on backend, you can start directly from (3) _____
- Use already ready verified RTL codes

⇨ implement one basic design from RTL to physical design to understand the entire VLSI (4) _____.

Level Three Projects

Ready open-source blocks include:

- Pico RV32 – RISC-V core
- AES block – 128 and 256 crypto core
- 32 × 32 or 64 × 64 MAC unit

Some blocks will be congestion critical and (5) _____ critical

The goal is to (6) _____ these designs.

LIVEWORKSHEETS