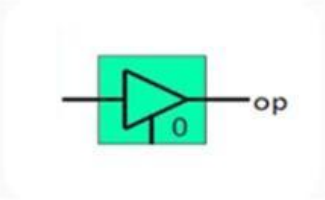
Mid-term examination

CPE-411: Advanced Digital Design

1. Which among the following is a process of transforming RTL to a gate-level netlist?
   A. Simulation
   B. Optimization
   C. Synthesis
   D. Verification

2. 

   The output of the following logic = ?
   A. 0
   B. 1
   C. X
   D. Z

3. #40 $finish indicates
   A. End of simulation time
   B. End of simulation at 40-time units
   C. Suspend simulation at 40-time units
   D. None

LIVEWORKSHEETS